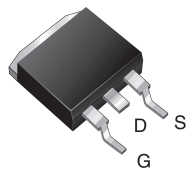
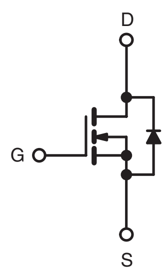
Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	200	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.80
Q_g (Max.) (nC)	16	
Q_{gs} (nC)	2.9	
Q_{gd} (nC)	9.6	
Configuration	Single	

SMD-220





N-Channel MOSFET

FEATURES

- Surface Mount
- Available in Tape and Reel
- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Logic Level Gate Drive
- $R_{DS(on)}$ Specified at V_{GS} = 4 V and 5 V
- Fast Switching
- Lead (Pb)-free Available

Available
RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.
The SMD-220 is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The SMD-220 is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

ORDERING INFORMATION		
Package	SMD-220	SMD-220
Lead (Pb)-free IRL620STRLPbF	IRL530SPbF	IRL620STRLPbF[a]
	SiH530S-E3	SiHL620STL-E3[a]
SnPb	IRL530STRR	-
	SiH530STR	-

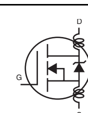
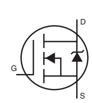
Note
a. See device orientation.

ABSOLUTE MAXIMUM RATINGS T_C = 25 °C, unless otherwise noted					
PARAMETER			**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage			V_{DS}	200	V
Gate-Source Voltage			V_{GS}	± 10	
Continuous Drain Current	V_{GS} at 5 V	T_C = 25 °C	I_D	5.2	A
		T_C = 100 °C		3.3	
Pulsed Drain Current[a]			I_{DM}	21	
Linear Derating Factor				0.40	W/°C
Linear Derating Factor (PCB Mount)[e]				0.025	
Single Pulse Avalanche Energy[b]			E_{AS}	125	mJ
Repetitive Avalanche Current[a]			I_{AR}	5.2	A
Repetitive Avalanche Energy[a]			E_{AR}	5.0	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	50	W
Maximum Power Dissipation (PCB Mount)[e]	T_A = 25 °C			3.1	
Peak Diode Recovery dV/dt[c]			dV/dt	5.0	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300[d]	

Notes
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. V_{DD} = 50 V, starting T_J = 25 °C, L = 6.9 mH, R_G = 25 Ω, I_{AS} = 5.2 A (see fig. 12).
c. $I_{SD} \leq$ 5.2 A, dI/dt $\leq$ 95 A/µs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 150 °C.
d. 1.6 mm from case.
e. When mounted on 1" square PCB (FR-4 or G-10 material).
* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to Ambient (PCB mount)[a]	R_{thJA}	-	40	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	2.5	

Note
a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	200	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA	-	0.27	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1.0	-	2.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 10 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 200 V, V_{GS} = 0 V	-	-	25	µA
		V_{DS} = 320 V, V_{GS} = 0 V, T_J = 125 °C	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10.0 V, I_D = 3.1 A[b]	-	-	0.80	Ω
		V_{GS} = 4.0 V, I_D = 2.6 A[b]	-	-	1.0	
Forward Transconductance	g_{fs}	V_{DS} = 50 V, I_D = 3.1 A[b]	1.2	-	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5	-	360	-	pF
Output Capacitance	C_{oss}		-	91	-	
Reverse Transfer Capacitance	C_{rss}		-	27	-	
Total Gate Charge	Q_g	V_{GS} = 5.0 V, I_D = 5.2 A, V_{DS} = 160 V, see fig. 6 and 13[b]	-	-	16	nC
Gate-Source Charge	Q_{gs}		-	-	2.9	
Gate-Drain Charge	Q_{gd}		-	-	9.6	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 100 V, I_D = 5.2 A, R_G = 9.0 Ω, R_D = 20 Ω, see fig. 10[b]	-	4.2	-	ns
Rise Time	t_r		-	31	-	
Turn-Off Delay Time	$t_{d(off)}$		-	18	-	
Fall Time	t_f		-	17	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal Source Inductance	L_S		-	7.5	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	5.2	A
Pulsed Diode Forward Current[a]	I_{SM}		-	-	21	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 5.2 A, V_{GS} = 0 V[b]	-	-	1.8	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 5.2 A, dI/dt = 100 A/µs[b]	-	180	270	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	1.1	1.7	µC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

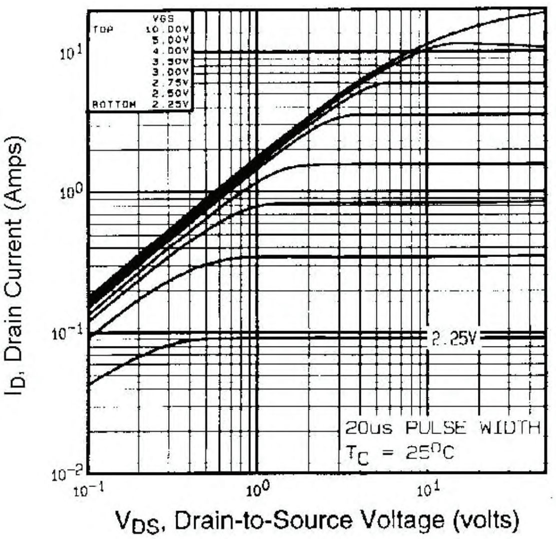


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

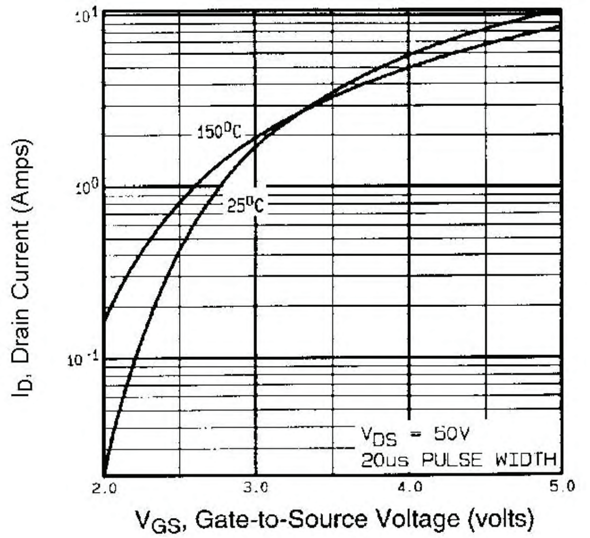


Fig. 3 - Typical Transfer Characteristics

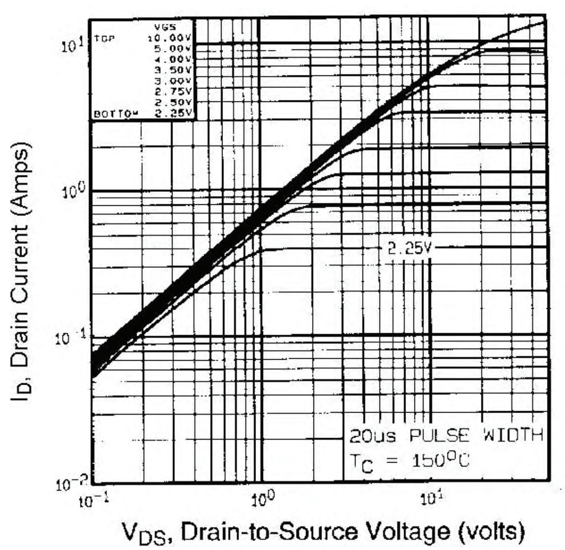


Fig. 2 - Typical Output Characteristics, T_C = 150 °C

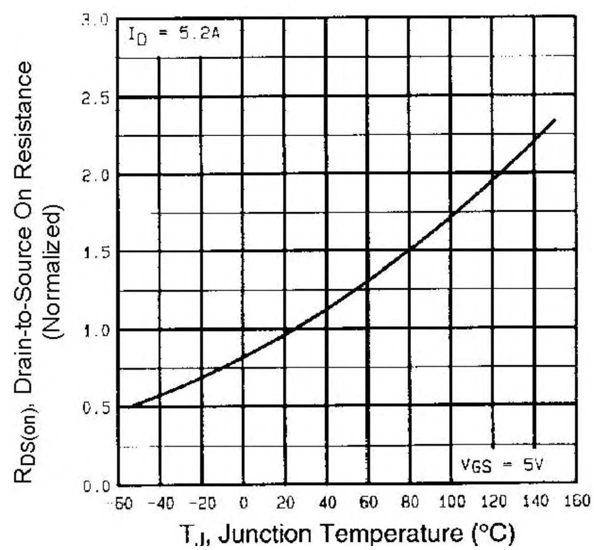


Fig. 4 - Normalized On-Resistance vs. Temperature

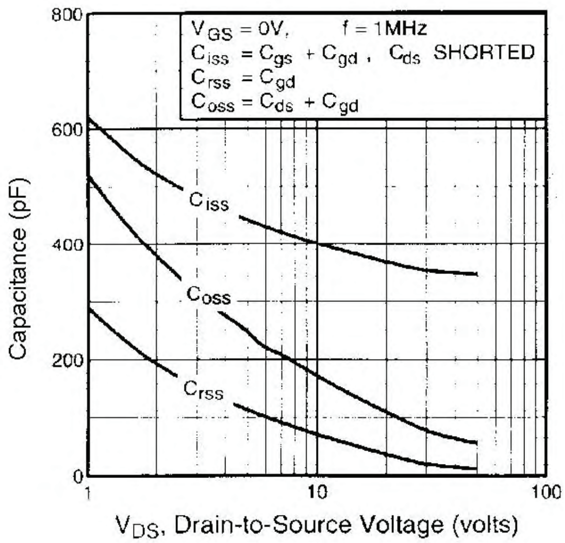


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

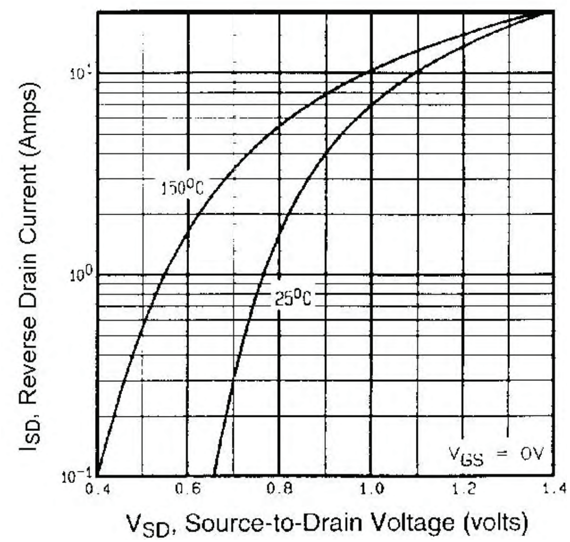


Fig. 7 - Typical Source-Drain Diode Forward Voltage

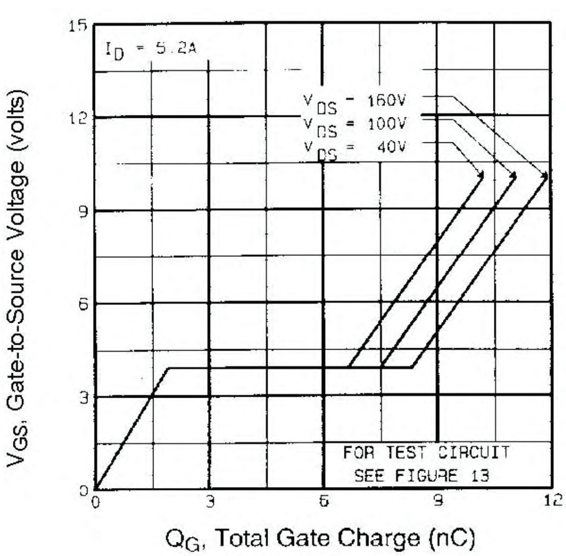


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

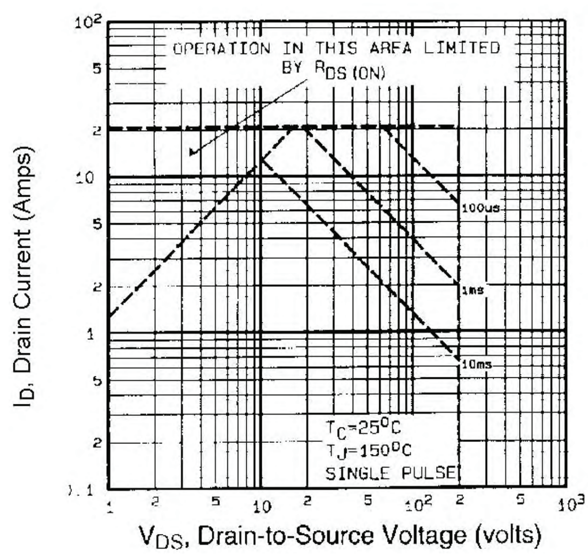


Fig. 8 - Maximum Safe Operating Area

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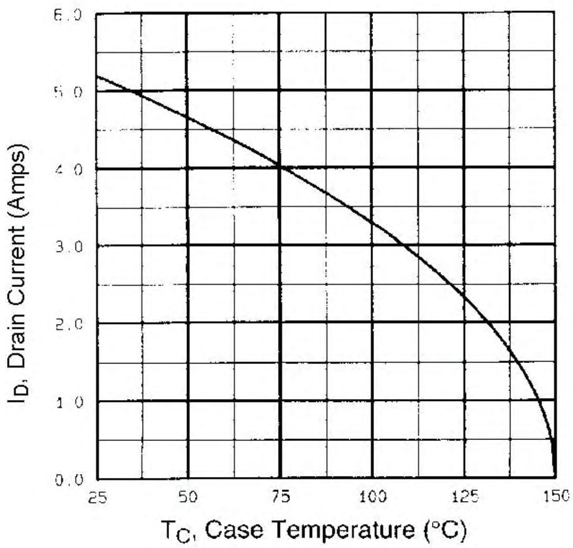


Fig. 9 - Maximum Drain Current vs. Case Temperature

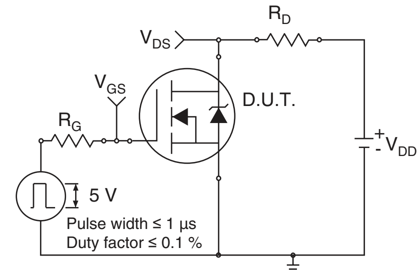


Fig. 10a - Switching Time Test Circuit

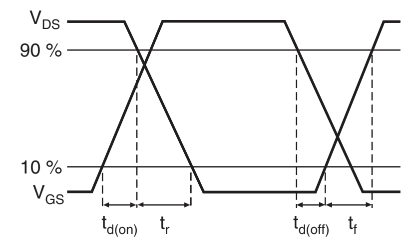


Fig. 10b - Switching Time Waveforms

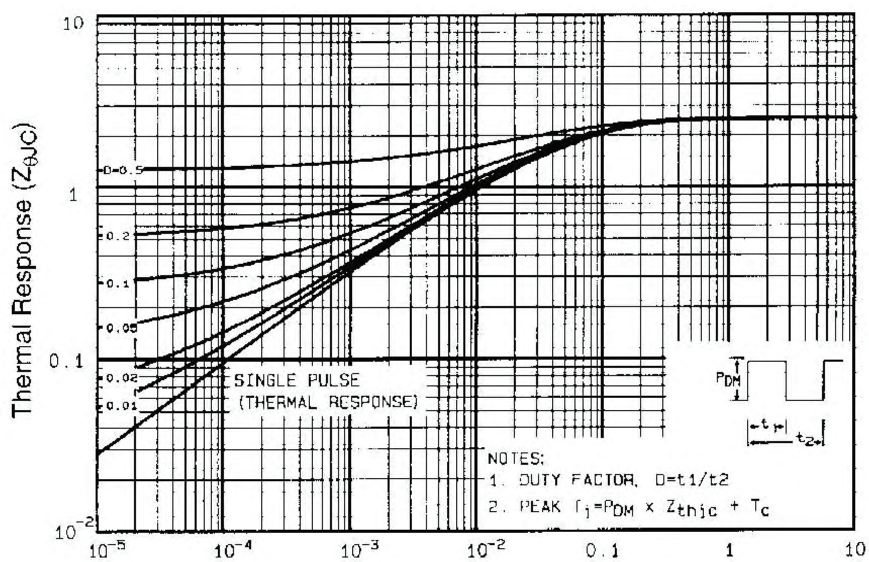


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

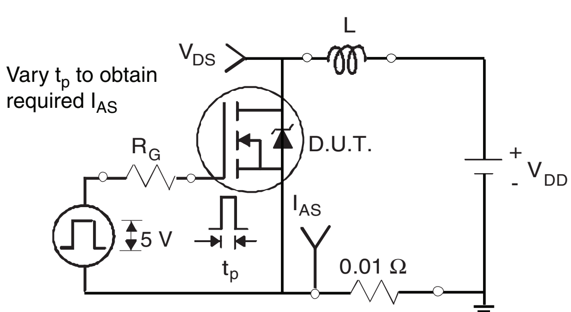


Fig. 12a - Unclamped Inductive Test Circuit

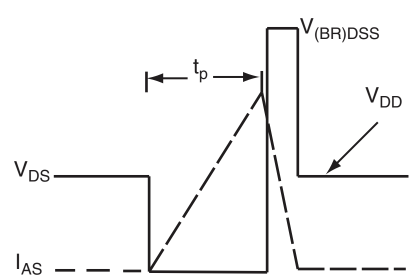


Fig. 12b - Unclamped Inductive Waveforms

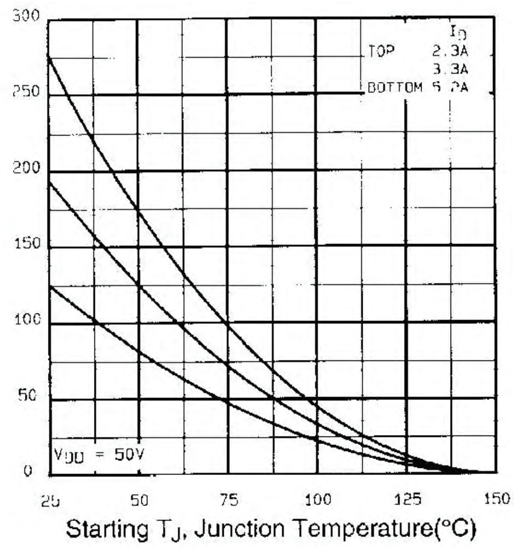


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

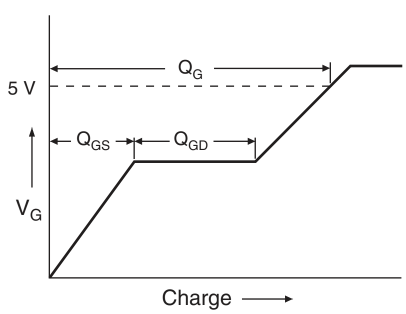


Fig. 13a - Basic Gate Charge Waveform

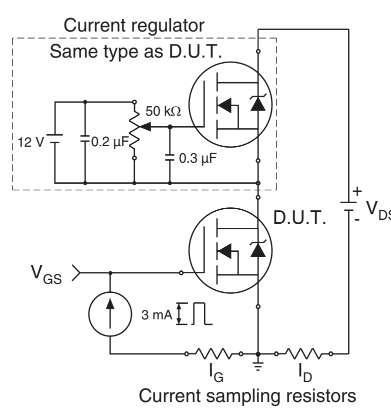
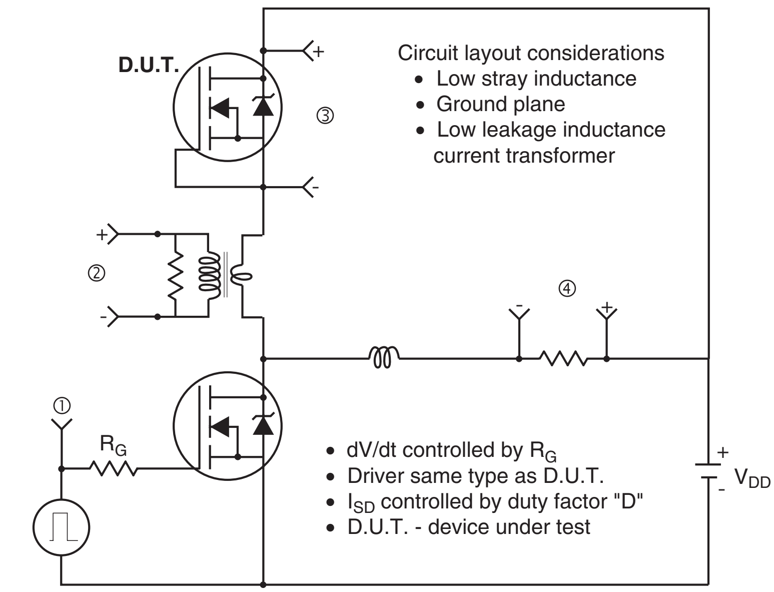


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



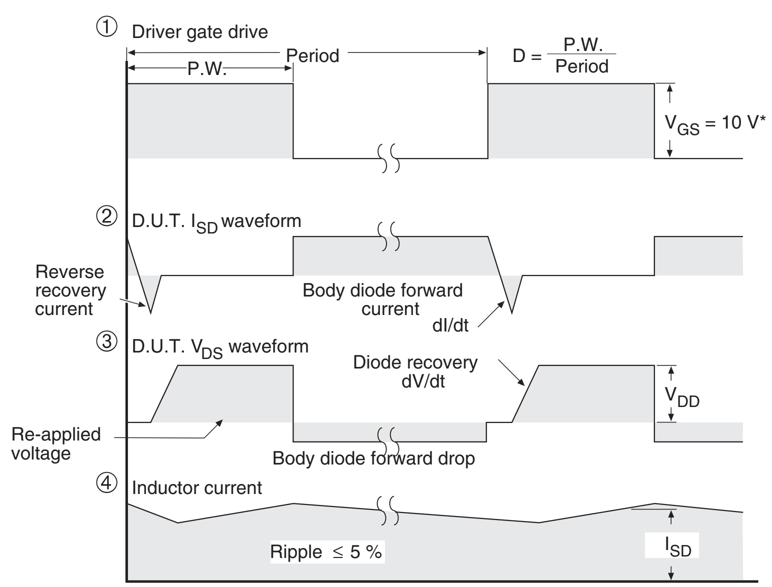


Fig. 14 - For N-Channel

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